

# OKI Semiconductor

## MSM5117805A

2,097,152-Word × 8-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

### DESCRIPTION

The MSM5117805A is a 2,097,152-word × 8-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM5117805A achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM5117805A is available in a 28-pin plastic SOJ or 28-pin plastic TSOP.

### FEATURES

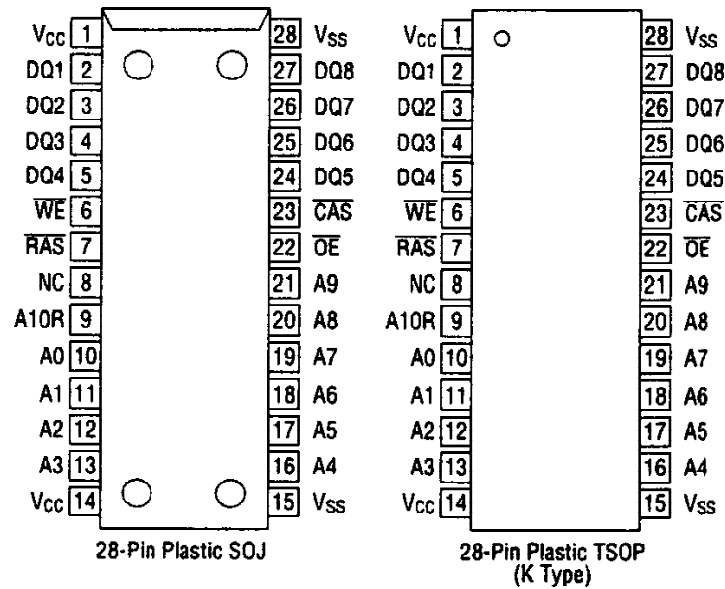
- 2,097,152-word × 8-bit configuration
  - Single 5 V power supply, ±10% tolerance
  - Input : TTL compatible, low input capacitance
  - Output : TTL compatible, 3-state
  - Refresh : 2048 cycles/32 ms
  - Fast page mode with EDO, read modify write capability
  - $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
  - Multi-bit test mode capability
  - Package options:
 

28-Pin 400 mil plastic SOJ	(SOJ28-P-400)	(Product : MSM5117805A-xxJS)
28-Pin 400 mil plastic TSOP	(TSOP28-P-400-K)	(Product : MSM5117805A-xxTS-K)
- xx indicates speed rank.

### PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>		Operating (Max.)	Standby (Max.)
MSM5117805A-60	60 ns	30 ns	15 ns	15 ns	110 ns	715 mW	5.5 mW
MSM5117805A-70	70 ns	35 ns	20 ns	20 ns	130 ns	660 mW	
MSM5117805A-80	80 ns	40 ns	20 ns	20 ns	150 ns	605 mW	

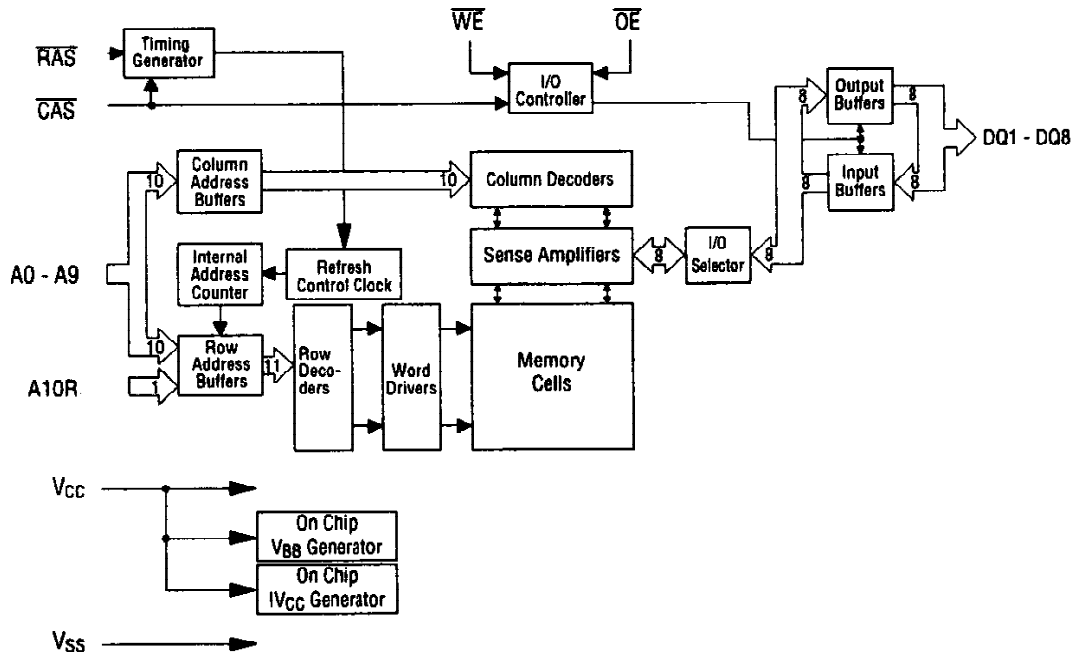
## PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0 - A9, A10R	Address Input
RAS	Row Address Strobe
CAS	Column Address Strobe
DQ1 - DQ8	Data Input/Data Output
$\overline{OE}$	Output Enable
WE	Write Enable
Vcc	Power Supply (5 V)
Vss	Ground (0 V)

Note : The same power supply voltage must be provided to every  $V_{CC}$  pin, and the same GND voltage level must be provided to every  $V_{SS}$  pin.

**BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>T</sub>	-1.0 to 7.0	V
Short Circuit Output Current	I <sub>OS</sub>	50	mA
Power Dissipation	P <sub>D</sub> *	1	W
Operating Temperature	T <sub>opr</sub>	0 to 70	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C

\*: T<sub>a</sub> = 25°C**Recommended Operating Conditions**(T<sub>a</sub> = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	—	6.5	V
Input Low Voltage	V <sub>IL</sub>	-1.0	—	0.8	V

**Capacitance**(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9, A10R)	C <sub>IN1</sub>	—	5	pF
Input Capacitance (RAS, CAS, WE, OE)	C <sub>IN2</sub>	—	7	pF
Output Capacitance (DQ1 - DQ8)	C <sub>I/O</sub>	—	7	pF

DC Characteristics

( $V_{CC} = 5V \pm 10\%$ ,  $T_a = 0^\circ C$  to  $70^\circ C$ )

Parameter	Symbol	Condition	MSM5117805 A-60		MSM5117805 A-70		MSM5117805 A-80		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	$V_{OH}$	$I_{OH} = -5.0\text{ mA}$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 4.2\text{ mA}$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	$I_{LI}$	$0V \leq V_I \leq 6.5V$ ; All other pins not under test = 0V	-10	10	-10	10	-10	10	$\mu A$	
Output Leakage Current	$I_{LO}$	DQ disable $0V \leq V_O \leq 5.5V$	-10	10	-10	10	-10	10	$\mu A$	
Average Power Supply Current (Operating)	$I_{CC1}$	$\overline{RAS}$ , $\overline{CAS}$ cycling, $t_{RC} = \text{Min.}$	—	130	—	120	—	110	mA	1, 2
Power Supply Current (Standby)	$I_{CC2}$	$\overline{RAS}$ , $\overline{CAS} = V_{IH}$ $\overline{RAS}$ , $\overline{CAS}$ $\geq V_{CC} - 0.2V$	—	2	—	2	—	2	mA	1
Average Power Supply Current ( $\overline{RAS}$ -only Refresh)	$I_{CC3}$	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ , $t_{RC} = \text{Min.}$	—	130	—	120	—	110	mA	1, 2
Power Supply Current (Standby)	$I_{CC5}$	$\overline{RAS} = V_{IH}$ , $\overline{CAS} = V_{IL}$ , DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ( $\overline{CAS}$ before $\overline{RAS}$ Refresh)	$I_{CC6}$	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	—	130	—	120	—	110	mA	1, 2
Average Power Supply Current (Fast Page Mode)	$I_{CC7}$	$\overline{RAS} = V_{IL}$ , $\overline{CAS}$ cycling, $t_{PC} = \text{Min.}$	—	120	—	110	—	100	mA	1, 3

- Notes :
1.  $I_{CC}$  Max. is specified as  $I_{CC}$  for output open condition.
  2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .
  3. Address can be changed once or less while  $\overline{CAS} = V_{IH}$ .

## AC Characteristics (1/2)

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C) Note 1, 2, 3, 12, 13

Parameter	Symbol	MSM5117805 A-60		MSM5117805 A-70		MSM5117805 A-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t <sub>RC</sub>	110	—	130	—	150	—	ns	
Read Modify Write Cycle Time	t <sub>RWC</sub>	150	—	180	—	200	—	ns	
Fast Page Mode Cycle Time	t <sub>HPC</sub>	25	—	30	—	35	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t <sub>PRWC</sub>	80	—	95	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t <sub>AA</sub>	—	30	—	35	—	40	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t <sub>CPA</sub>	—	35	—	40	—	45	ns	4
Access Time from $\overline{\text{OE}}$	t <sub>OEA</sub>	—	15	—	20	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t <sub>CLZ</sub>	0	—	0	—	0	—	ns	4
Data Output Hold After $\overline{\text{CAS}}$ Low	t <sub>DOH</sub>	3	15	3	15	3	15	ns	
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t <sub>CEZ</sub>	3	15	3	15	3	15	ns	7, 8
$\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time	t <sub>REZ</sub>	3	15	3	15	3	15	ns	7, 8
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t <sub>OEZ</sub>	3	15	3	15	3	15	ns	7
$\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time	t <sub>WEZ</sub>	3	15	3	15	3	15	ns	7
Transition Time	t <sub>T</sub>	3	50	3	50	3	50	ns	3
Refresh Period	t <sub>REF</sub>	—	32	—	32	—	32	ms	
$\overline{\text{RAS}}$ Precharge Time	t <sub>RP</sub>	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode with EDO)	t <sub>RASP</sub>	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	15	—	20	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t <sub>ROH</sub>	15	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode with EDO)	t <sub>CP</sub>	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t <sub>CAS</sub>	10	10,000	10	10,000	15	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	40	—	45	—	50	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>CRP</sub>	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>RHCP</sub>	35	—	40	—	45	—	ns	
$\overline{\text{OE}}$ Hold Time from $\overline{\text{CAS}}$ (DQ Disable)	t <sub>CHO</sub>	5	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t <sub>RCD</sub>	20	45	20	50	20	60	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t <sub>RAD</sub>	15	30	15	35	15	40	ns	6
$\overline{\text{RAS}}$ to Second $\overline{\text{CAS}}$ Delay Time	t <sub>RSCD</sub>	60	—	70	—	80	—	ns	
Row Address Set-up Time	t <sub>ASR</sub>	0	—	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	10	—	10	—	10	—	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	—	0	—	0	—	ns	
Column Address Hold Time	t <sub>CAH</sub>	15	—	15	—	15	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t <sub>AR</sub>	40	—	45	—	50	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	30	—	35	—	40	—	ns	

AC Characteristics (2/2)

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C) Note 1, 2, 3, 12, 13

Parameter	Symbol	MSM5117805 A-60		MSM5117805 A-70		MSM5117805 A-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—	0	—	ns	
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	0	—	ns	9
Read Command Hold Time referenced to RAS	t <sub>RBH</sub>	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	0	—	ns	10
Write Command Hold Time	t <sub>WCH</sub>	10	—	15	—	15	—	ns	
Write Command Hold Time from RAS	t <sub>WCR</sub>	40	—	45	—	50	—	ns	
Write Command Pulse Width	t <sub>WP</sub>	10	—	15	—	15	—	ns	
WE Pulse Width (DQ Disable)	t <sub>WPE</sub>	5	—	10	—	10	—	ns	
OE Command Hold Time	t <sub>OEH</sub>	15	—	20	—	20	—	ns	
OE Precharge Time	t <sub>OEP</sub>	10	—	10	—	10	—	ns	
OE Command Hold Time	t <sub>OCH</sub>	10	—	10	—	10	—	ns	
Write Command to RAS Lead Time	t <sub>RWL</sub>	15	—	20	—	20	—	ns	
Write Command to CAS Lead Time	t <sub>CWL</sub>	15	—	20	—	20	—	ns	
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	0	—	ns	11
Data-in Hold Time	t <sub>DH</sub>	15	—	15	—	15	—	ns	11
Data-in Hold Time from RAS	t <sub>DHR</sub>	40	—	45	—	50	—	ns	
OE to Data-in Delay Time	t <sub>OED</sub>	15	—	15	—	15	—	ns	
CAS to WE Delay Time	t <sub>CWD</sub>	35	—	45	—	45	—	ns	10
Column Address to WE Delay Time	t <sub>AWD</sub>	50	—	60	—	65	—	ns	10
RAS to WE Delay Time	t <sub>RWD</sub>	80	—	95	—	105	—	ns	10
CAS Precharge WE Delay Time	t <sub>CPWD</sub>	55	—	65	—	70	—	ns	10
CAS Active Delay Time from RAS Precharge	t <sub>RPC</sub>	5	—	5	—	5	—	ns	
RAS to CAS Set-up Time (CAS before RAS)	t <sub>CSR</sub>	5	—	5	—	5	—	ns	
RAS to CAS Hold Time (CAS before RAS)	t <sub>CHR</sub>	10	—	15	—	15	—	ns	
CAS Precharge Time (Refresh Counter Test)	t <sub>CPT</sub>	20	—	30	—	40	—	ns	
WE to RAS Precharge Time (CAS before RAS)	t <sub>WRP</sub>	10	—	10	—	10	—	ns	
WE Hold Time from RAS (CAS before RAS)	t <sub>WRH</sub>	10	—	10	—	10	—	ns	
RAS to WE Set-up Time (Test Mode)	t <sub>WTS</sub>	10	—	10	—	10	—	ns	
RAS to WE Hold Time (Test Mode)	t <sub>WTH</sub>	10	—	10	—	10	—	ns	

- Notes:
1. A start-up delay of 200  $\mu$ s is required after power-up, followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 5$  ns.
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, access time is controlled by  $t_{AA}$ .
  7.  $t_{CEZ}$  (Max.),  $t_{REZ}$  (Max.),  $t_{WEZ}$  (Max.) and  $t_{OEZ}$  (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{CEZ}$  and  $t_{REZ}$  must be satisfied for open circuit condition.
  9.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  10.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (Min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}$  (Min.),  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{AWD} \geq t_{AWD}$  (Min.) and  $t_{CPWD} \geq t_{CPWD}$  (Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  11. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in an early write cycle, and to  $\overline{\text{WE}}$  leading edge in an  $\overline{\text{OE}}$  control write cycle or a read modify write cycle.
  12. The test mode is initiated by performing a  $\overline{\text{WE}}$  and  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA9 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a  $\overline{\text{RAS}}$ -only refresh cycle or a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle.
  13. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

**See ADDENDUM L for AC Timing Waveforms**